



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,034	03/30/2004	Wilco Dijkstra	550-518	1420
23117	7590	08/15/2006	EXAMINER	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			FIEGLE, RYAN PAUL	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/812,034	DIJKSTRA, WILCO
	Examiner	Art Unit
	Ryan P. Fiegler	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 21 July 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-31 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-31 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Specification and Drawings

1. The amendments to the drawings are noted and accepted.
2. The amended title refers to "multiple register files." The present invention actually only contains one register file, the transfer takes place between multiple registers *in* that register file. Besides this aspect, the amended title looks acceptable.

Claim Rejections - 35 USC § 101

3. The examiner gratefully acknowledges and accepts the amendments to the claims to remedy the 101 problems.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1. Claims 1, 2, 8, 9, 11, 12, 18, 19, 21, 22, 28 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Huck et al. (US Patent 6,408,380).

2. As per claim 1:

A data processing apparatus, comprising:
a data processing unit operable to perform data processing operations on data values (Figure 4, item 402);
a register file having a plurality of registers operable to store said data values for access by the data processing unit (Figure 4, item 416);
the data processing unit being responsive to a single transfer instruction to perform multiple data value transfers between a corresponding multiple of said registers of said register file and consecutive data value addresses in a memory, the single transfer instruction providing an address identifier from which said consecutive data value addresses are derivable, and further providing for each of said data value transfers a register identifier identifying the register within said plurality of registers which is the subject of that data value transfer, said register identifier for each of said data value transfers being specifiable independently of the register identifiers specified for the other of said data value transfers (Abstract; column 2, lines 53-61).

3. As per claim 2:

A data processing apparatus as claimed in claim 1, wherein said single transfer instruction is a load instruction, the data processing unit being responsive to the load instruction to perform said multiple data value transfers from the consecutive data value addresses in said memory to said corresponding multiple of said registers of said register file (Abstract; column 2, lines 53-61).

4. As per claim 8:

A data processing apparatus as claimed in claim 1, wherein the data processing unit is responsive to the single transfer instruction to perform two data value transfers (Abstract).

5. As per claim 9:

A data processing apparatus as claimed in claim 1, wherein each of said data values comprise a 32-bit data word, and said consecutive data value addresses identify addresses for a series of adjacent 32-bit data words in the memory (column 1, lines 15-18).

6. As per claim 11:

A method of operating a data processing apparatus to transfer data values between a register file and a memory, the register file having a plurality of registers operable to store said data values for access by a data processing unit operable to perform data processing operations on said data values, the method comprising the steps of:

in response to a single transfer instruction, performing multiple data value transfers between a corresponding multiple of said registers of said register file and consecutive data value addresses in a memory by (Abstract; column 2, lines 53-61):

deriving said consecutive data value addresses from an address identifier provided by the single transfer instruction (Abstract; column 2, lines 53-61);

determining for each of said data value transfers, with reference to a corresponding register identifier provided by said single transfer instruction, the register within said plurality of registers which is the subject of that data value transfer, the

register identifier for each of said data value transfers being specifiable independently of the register identifiers specified for the other of said data value transfers (Abstract; column 2, lines 53-61); and

performing the multiple data value transfers (Abstract; column 2, lines 53-61).

7. As per claims 12, 18 and 19:

Claims 12, 18 and 19 claim the method of running the apparatus of claims 2, 8 and 9 and are rejected for the same reasons.

8. As per claims 21, 22, 28 and 29:

Claims 21, 22, 28 and 29 claim a computer program to run the method of claims 11, 12, 18 and 19. Such is disclosed by Huck (column 2, lines 43-45).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 7-9, 11-15, 17-19 and 21-25 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hitt (US Patent 3,654,448) in view of Huck (US Patent 6,408,380).

10. As per claim 1:

Hitt teaches a data processing apparatus, comprising:

a data processing unit operable to perform data processing operations on data values (Hitt: column 4, lines 60-70);

a register file having a plurality of registers operable to store said data values for access by the data processing unit (Hitt: column 4, lines 60-70);

the data processing unit being responsive to a single transfer instruction to perform multiple data value transfers between a corresponding multiple of said registers of said register file and consecutive data value addresses in a memory, the single transfer instruction providing an address identifier from which said consecutive data value addresses are derivable, and further providing for each of said data value transfers a register identifier identifying the register within said plurality of registers which is the subject of that data value transfer (Hitt: column 4, lines 60-70).

Hitt does not teach said register identifier for each of said data value transfers being specifiable independently of the register identifiers specified for the other of said data value transfers while Huck does (Abstract).

Huck states that Hitt's method is at a disadvantage because it is limited to consecutive registers (Huck: column 1, line 65 to column 2, line 5).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Huck to Hitt would give Hick the advantage of referring to nonconsecutive registers.

11. As per claim 2:

A data processing apparatus as claimed in claim 1, wherein said single transfer instruction is a load instruction, the data processing unit being responsive to the load

instruction to perform said multiple data value transfers from the consecutive data value addresses in said memory to said corresponding multiple of said registers of said register file (Hitt: column 4, lines 70-75).

12. As per claim 3:

A data processing apparatus as claimed in claim 1, wherein said single transfer instruction is a store instruction, the data processing unit being responsive to the store instruction to perform said multiple data value transfers from said corresponding multiple of said registers of said register file to the consecutive data value addresses in said memory (Hitt: column 4, line 70; column 5, lines 1-3).

13. As per claim 4:

A data processing apparatus as claimed in claim 1, wherein the address identifier comprises a base address and an offset value (Hitt: column 4, lines 45-48).

14. As per claim 5:

A data processing apparatus as claimed in claim 4, wherein the base address is specified within the single transfer instruction by a base address register identifier identifying one of said plurality of registers that is arranged to store the base address (Hitt: column 4, lines 45-48; column 4, line 70; column 5, lines 1-3).

15. As per claim 7:

A data processing apparatus as claimed in claim 4, wherein the offset value is specified by an immediate value provided within the single transfer instruction (Hitt: column 4, lines 45-48).

16. As per claim 8:

A data processing apparatus as claimed in claim 1, wherein the data processing unit is responsive to the single transfer instruction to perform two data value transfers (Hitt: column 4, lines 60-66) (The registers are capable of having a span of 2).

17. As per claim 9:

A data processing apparatus as claimed in claim 1, wherein each of said data values comprise a 32-bit data word, and said consecutive data value addresses identify addresses for a series of adjacent 32-bit data words in the memory (Hitt: column 4, line 40) (The fact that the instructions are 32 bits means that it is inherent that it is a 32-bit architecture and therefore the data will be 32 bits.).

18. As per claim 11:

A method of operating a data processing apparatus to transfer data values between a register file and a memory, the register file having a plurality of registers operable to store said data values for access by a data processing unit operable to perform data processing operations on said data values, the method comprising the steps of:

in response to a single transfer instruction, performing multiple data value transfers between a corresponding multiple of said registers of said register file and consecutive data value addresses in a memory by (Hitt: column 4, lines 60-70):

deriving said consecutive data value addresses from an address identifier provided by the single transfer instruction (Hitt: column 4, lines 60-70);

determining for each of said data value transfers, with reference to a corresponding register identifier provided by said single transfer instruction, the register within said plurality of registers which is the subject of that data value transfer, performing the multiple data value transfers (Hitt: column 4, lines 60-70).

Hitt does not teach said register identifier for each of said data value transfers being specifiable independently of the register identifiers specified for the other of said data value transfers while Huck does (Huck: Abstract).

Huck states that Hitt's method is at a disadvantage because it is limited to consecutive registers (Huck: column 1, line 65 to column 2, line 5).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Huck to Hitt would give Hick the advantage of referring to nonconsecutive registers.

19. As per claims 12-15 and 17-19:

Claims 12-15 and 17-19 claim the method of running the apparatus of claims 2-5 and 7-9 and are rejected for the same reasons.

20. As per claims 21-25 and 27-29:

Claims 21-25 and 27-29 claim a computer program to run the method of claims 11-15 and 17-19. Though not explicitly disclosed by Hitt, such is inherent for Hitt's system to be able to complete the method disclosed. Therefore, claims 21-25 and 27-29 are rejected for the same reasons as claims 11-15 and 17-19.

21. Claims 6, 10, 16, 20, 26 and 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hitt and Huck as applied to claims 1, 11 and 21 above.

22. As per claim 6:

Hitt does not teach the data processing apparatus as claimed in claim 4, wherein the offset value is specified within the single transfer instruction by an offset register identifier identifying one of said plurality of registers that is arranged to store the offset value (Hitt: column 4, lines 40-48).

Official Notice is taken in that it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to make the offset available in a register rather than in an immediate field if there were advantages to doing so. For instance, if Hitt was updated for a present day system where there were 64 addressable architectural registers rather than 16, then 6 bits would be needed for each register reference. With Hitt's present setup, that would take 18 bits for register addressing plus the 8 for the opcode, for 26 total bits. This only leaves 6 bits for the offset, which only gives a square root of the offset addressability as Hitt's original instruction. However, this is just enough bits to address another register, which would be made to hold the offset. Therefore, in an updated system, storing the offset in a register rather than keeping it in an immediate field would allow Hitt to address 4x registers and 1048576x more addresses to add to the base address.

23. Claims 16 and 26 are rejected for the same reasons as claim 6.

24. As per claim 10:

Hitt does not teach a data processing apparatus as claimed in claim 1, further comprising an interface between said register file and said memory which facilitates the performance of said multiple data value transfers in parallel.

Official notice is taken in that it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention to perform the data transfers in parallel in a modern day system since the address calculation is very simple and would save execution time without much additional logic. For example, in Hitt's worst-case scenario, the LM instruction will take 16 cycles, where if the transfers were done in parallel, this would be cut down to 1 cycle.

25. Claims 20 and 30 are rejected for the same reasons as claim 10.

26. As per claims 31:

Hitt does not teach a computer program operable to configure a data processing apparatus to perform a method as claimed in claim 11.

While such a computer program would be inherent in present day systems since it would be impossible to configure such a device by hand using modern < 90nm technology, such can not be inferred in Hitt since it was published in 1972. In all probability, the system was configured by hand.

However, one of ordinary skill in the pertinent art at the time of the applicant's invention would have recognized that if Hitt was modernized, it would have to be configured by a machine, and therefore a computer program would be needed to run that computer. Further, in reference to claim 32, it would have been obvious that this program needs to be encapsulated by some medium to be stored.

Response to Arguments

27. Applicant's arguments, see paragraph 2 of page 4 of the remarks, filed 7/21/06, with respect to the rejection(s) of claim(s) 1, 11 and 21 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Huck and a combination of Hitt and Huck. Because these rejections have not been necessitated by amendment, this action is made non-final.

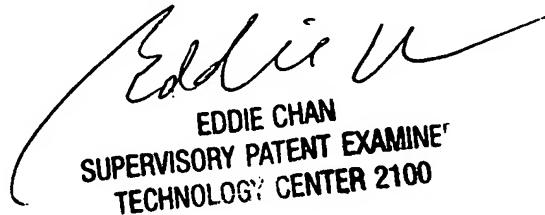
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
Art Unit 2183



EDDIE CHAN
SUPERVISORY PATENT EXAMINE^r
TECHNOLOGY CENTER 2100